FORCE MEASURING SYSTEM FOR A LONG SPAN STRUCTURAL FRAME

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Abstract. *The civil engineering industry seeks each day the improvement in its productive processes. To be able to perform tests in real size structural elements at the laboratory, it becomes necessary the use of a robust structure, that is able to resist the huge strains in action during the tests. This structure is called Loan Span Structural Frame (LSSF), being made usually of heavy steel I-girders, forming a closed structure of action and response. However, to be able to know the force that is being applied to the specimens test, there is the necessity of the instantaneous measurement of this force. The purpose of this article is to mold and develop a force measuring system (FMS) for a LSSF, with the features of measuring and analysis of experiments with prototypes of reinforced concrete beams, slabs and wall prisms of real size, allied to a lower cost of construction and maintenance, incorporating the appropriate technology to the creation of products, processes and/or prototypes in the civil construction area. The LSSF is being developed within a same research thematic project through a simultaneous engineering paradigm. The FMS developed for the LSSF, follows the basic principles of every measuring system, which are: the primary transducer (load cell), the signal conditioning and the signal presentation. The load cell used in the system utilizes the principle of conversion through LVDT (Linear Variable Differential Transformer). The signal conditioning system developed adjusts the offset of the output signal of the load cell, which presents a signal range of 0-20mV, and adjusts the gain that is applied to this signal, converting it to a 0-5V range, which will later be sent to a digital system of acquisition, encoding and transmission (DSAET). The communication with the computer is realized through software embedded in the DSAET. The presentation software was developed in C#.NET and works in proprietary platform. Through it, the measured signal is stored, analyzed and presented to the user. The research method proposed presents two stages. The first stage aggregates the requirements analysis for the system modeling phase, testing and model validation. The second stage comprehends the requirements analysis for implementation phase, system development, testing and validation through system calibration. For the last phase, the conclusion of the LSSF construction is expected. Preliminary tests have been made with the measuring system, aiming to adjust its working parameters. The FMS has the advantages of being exact, precise, cheap and adjusted to the necessities of the LSSF. The development of new methods and structure testing techniques are future goals.*

Keywords*: Structural Frame, Force Measuring System, Load Cell, Digital Signal Processing*

1. INTRODUCTION

The civil engineering industry seeks each day the improvement in its productive processes, specially the characteristics of the materials used and project parameters, allied to the always growing need for lower costs. In the engineering field, the use of measuring instruments is a necessary condition to achieve practical results in an unquestionable manner. To be able to perform tests in real size structural elements at the laboratory, it becomes necessary the use of a robust structure, that is able to resist the high loads in action during the tests.

There is a kind of structure, called Loan Span Structural Frame (LSSF) that is able to perform such tests in real size specimens. The LSSF is made usually of heavy steel I-girders, forming a closed structure of action and response. A specimens test fixed to the LSSF receives loads from a hydraulic jack, and the system makes it possible to obtain characteristics of rigidity and hardness of the tested elements.

By now, a LSSF is been developed at the Laboratory of Materials and Structures at UTFPR – Universidade Tecnológica Federal do Paraná, Brazil. Figure 1 and Fig. 2 shows the LSSF's structure been developed and Fig. 3 shows an overview of the LSSF. The LSSF will enable a 3 meters span for measuring and analysis of experiments with prototypes of reinforced concrete beams, slabs and wall prisms of real size, allied to a lower cost of construction and maintenance, incorporating the appropriate technology to the creation of products, processes and/or prototypes in the civil construction area.

Figure 1. LSSF's structure been developed

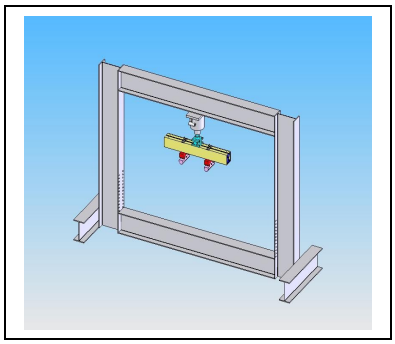

Figure 2. Overview of the LSSF

2. MEASURING SYSTEM

The LSSF needs a measuring system to converting mechanical force in electrical signal to be measured and presented in graphical mode in computers. To achieve this goal, is necessary to develop electronic circuits to conditioning, filtering, converting and presenting the magnitude of physical variables measured. The measuring system stages developed for this work was conditioning, converting and presenting, respectively. Figure 3 shows the block diagram of measuring system developed according to modern concepts of measuring systems (BALBINOT, 2007).

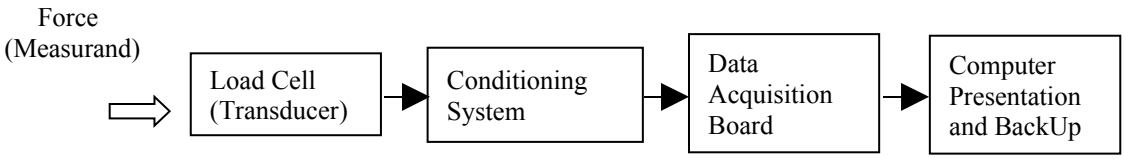

Figure 3. Measuring System Block Diagram

2.1. Load Cell Characteristics

The load cell used in this work is an EMIC 60TF cell, manufactured by EMIC. The functional principle of this load cell is based on LVDT (BEIHOFF, 1996). The voltage output range is 0-20mV and the maximal force measured is 60.000kg. The load cell can be seen in Fig. 4.

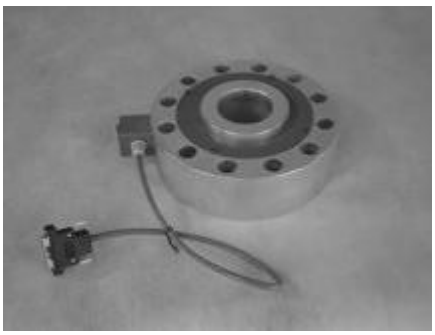

Figure 4. Load Cell EMIC60TF

The LVDT load cell principle of operation is based on movement of the core in the LVDT. As the core moves within the LVDT coil, the output of the coil varies with the core movement, which varies directly with the force F. The output is thus proportional to F. Figure 5 illustrates this principle of operation.

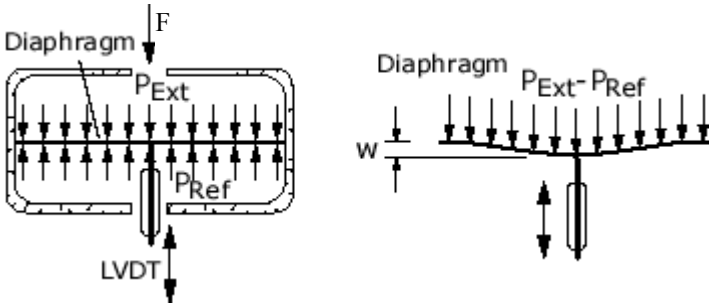

Figure 5. Diagram of LVDT Load Cell Operation

2.2. Signal Conditioning Circuit

Considering that conditioning system developed should provide a (0-5V) signal to a digital acquisition board, the maximal voltage output of conditioning system must be 5V. Therefore, to 0-20mV signal conditioning input variation must correspond to 0-5V signal conditioning output variation. Figure 6 shows the electronic circuit of the conditioning. This circuit contains an offset adjust to minimizes any possible load cell displacement. Also has stages for given gain to the input voltage signal to suit the range of the output voltage range (0-5V).

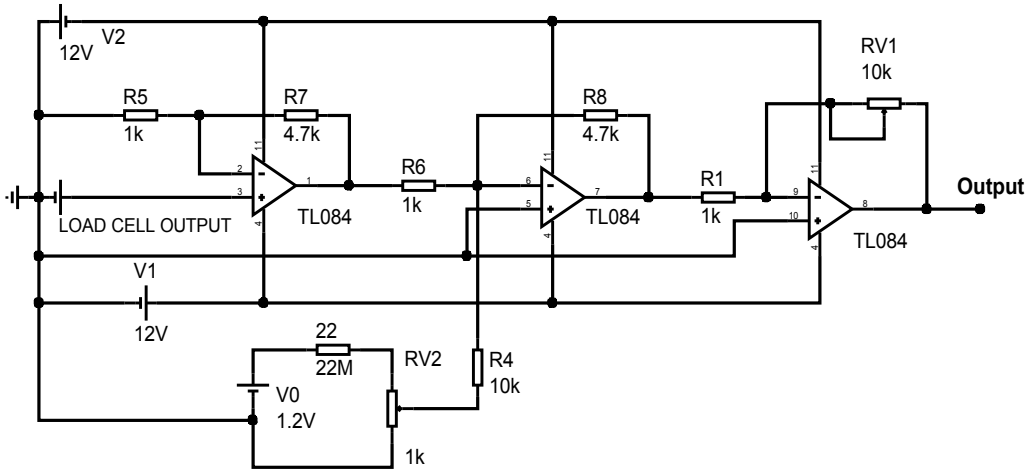

Figure 6. Signal Conditioning Electronic Circuit

The voltage gain was adjusted to obtain the best common mode rejection ratio (CMRR). Also, the input signal must be adjusted through a trimpot to minimize load cell errors propagating to later stages of measuring systems.

Table 1 shows the results obtained through Fig. 6 circuit simulation. The load cell output values were varied with step equal to 0.5 mV. The load cell output voltage simulated values were obtained with a virtual voltmeter with internal resistance of 1GΩ. Also shown are the calculated theoretical values for each value of the corresponding input, considering for these values, null error and linear output. Deviations are calculated for simulated output.

The theoretic and simulated output deviation in absolute and relative values are given by Eq. (1), Eq. (2) and Eq. (3), respectively:

$$\gamma = \alpha - \beta \tag{1}$$

$$\delta = (\alpha - \beta)/\alpha \tag{2}$$

$$\eta = [(\alpha - \beta)/\alpha].100 \tag{3}$$

where:

$\alpha = theoretical\ output\ value$

$\beta = simulated\ output\ value$

$\gamma = output\ deviation\ value$

$\delta = output\ relative\ deviation\ value$

$\eta = percentage\ output\ relative\ deviation\ value$

Table 1. Calculated and simulated values voltage signals and deviations.

Simulated Input (mV)	β (V)	α (V)	$\gamma = \alpha - \beta$	$\delta = (\alpha - \beta)/\alpha$	$\eta = [(\alpha - \beta)/\alpha].100$
0,00	0,0044190000	0,0000000001(1)	-0,0044189999	-0,0440000000	-4,4
0,50	0,1289750000	0,1250000000	-0,0039750000	-0,0318000000	-3,18
1,00	0,2535300000	0,2500000000	-0,0035300000	-0,0141200000	-1,41
1,50	0,3780860000	0,3750000000	-0,0030860000	-0,0082293333	-0,82
2,00	0,5026420000	0,5000000000	-0,0026420000	-0,0052840000	-0,53
2,50	0,6271980000	0,6250000000	-0,0021980000	-0,0035168000	-0,35
3,00	0,7517530000	0,7500000000	-0,0017530000	-0,0023373333	-0,23
3,50	0,8763090000	0,8750000000	-0,0013090000	-0,0014960000	-0,15
4,00	1,0010000000	1,0000000000	-0,0010000000	-0,0010000000	-0,1
4,50	1,1250000000	1,1250000000	0,0000000000	0,0000000000	0
5,00	1,2500000000	1,2500000000	0,0000000000	0,0000000000	0
5,50	1,3750000000	1,3750000000	0,0000000000	0,0000000000	0
6,00	1,4990000000	1,5000000000	0,0010000000	0,0006666667	0,07
6,50	1,6240000000	1,6250000000	0,0010000000	0,0006153846	0,06
7,00	1,7480000000	1,7500000000	0,0020000000	0,0011428571	0,11
7,50	1,8730000000	1,8750000000	0,0020000000	0,0010666667	0,11
8,00	1,9970000000	2,0000000000	0,0030000000	0,0015000000	0,15
8,50	2,1220000000	2,1250000000	0,0030000000	0,0014117647	0,14
9,00	2,2460000000	2,2500000000	0,0040000000	0,0017777778	0,18
9,50	2,3710000000	2,3750000000	0,0040000000	0,0016842105	0,17
10,00	2,4960000000	2,5000000000	0,0040000000	0,0016000000	0,16
10,50	2,6200000000	2,6250000000	0,0050000000	0,0019047619	0,19
11,00	2,7450000000	2,7500000000	0,0050000000	0,0018181818	0,18
11,50	2,8690000000	2,8750000000	0,0060000000	0,0020869565	0,21
12,00	2,9940000000	3,0000000000	0,0060000000	0,0020000000	0,2
12,50	3,1180000000	3,1250000000	0,0070000000	0,0022400000	0,22
13,00	3,2430000000	3,2500000000	0,0070000000	0,0021538462	0,22
13,50	3,3670000000	3,3750000000	0,0080000000	0,0023703704	0,24
14,00	3,4920000000	3,5000000000	0,0080000000	0,0022857143	0,23
14,50	3,6170000000	3,6250000000	0,0080000000	0,0022068966	0,22
15,00	3,7410000000	3,7500000000	0,0090000000	0,0024000000	0,24

15,50	3,8660000000	3,8750000000	0,0090000000	0,0023225806	0,23
16,00	3,9900000000	4,0000000000	0,0100000000	0,0025000000	0,25
16,50	4,1150000000	4,1250000000	0,0100000000	0,0024242424	0,24
17,00	4,2390000000	4,2500000000	0,0110000000	0,0025882353	0,26
17,50	4,3640000000	4,3750000000	0,0110000000	0,0025142857	0,25
18,00	4,4880000000	4,5000000000	0,0120000000	0,0026666667	0,27
18,50	4,6130000000	4,6250000000	0,0120000000	0,0025945946	0,26
19,00	4,7380000000	4,7500000000	0,0120000000	0,0025263158	0,25
19,50	4,8620000000	4,8750000000	0,0130000000	0,0026666667	0,27
20,00	4,9870000000	5,0000000000	0,0130000000	0,0026000000	0,26
20,05	4,9990000000	5,0125000000	0,0135000000	0,0026932668	0,27

(1): This value was modified to avoid division by zero during calculations. The real value is zero.

The graphs showed in Fig. 7 represents the circuit output simulated for conditioning real and theoretical output signals, respectively.

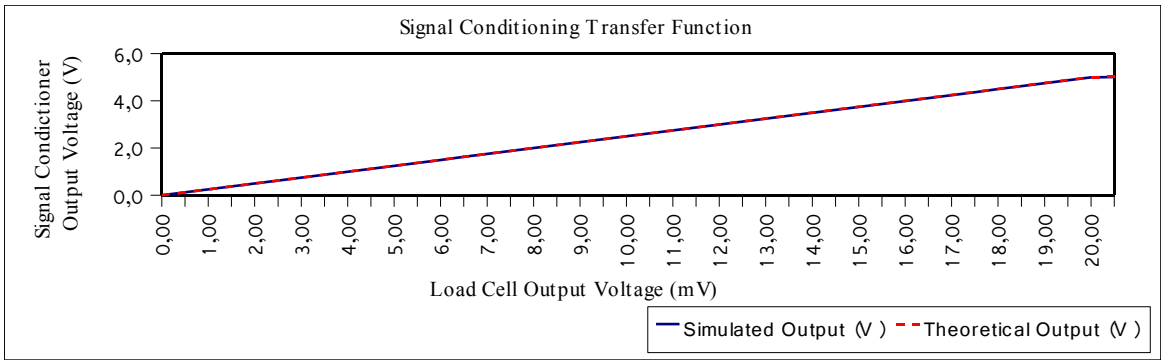

Figure 7. Signal Conditioning Transfer Function

The system presents an deviation on the initial range of measuring. The deviation simulated is about 4,4mV. It is perceived clearly that the deviation at the beginning of the scale is due to system resolution and the "tiny" nature of the output load cell voltage, i.e. it is impossible to perceive any change in output for very small signal input with this conditioning circuit. It carries a propagation error at the beginning of the scale. However, the deviation will be greater focus from the center to full-scale and the largest deviation found at the beginning of the scale. Figure 8 shows the output deviation value calculated versus load cell output voltage.

The simulated output, takes into account the differences related to theoretical and simulated output values. This value is also represented in percentage, see Fig. 9. Note that the largest deviation found for the signal conditioner is next to 4,4%.

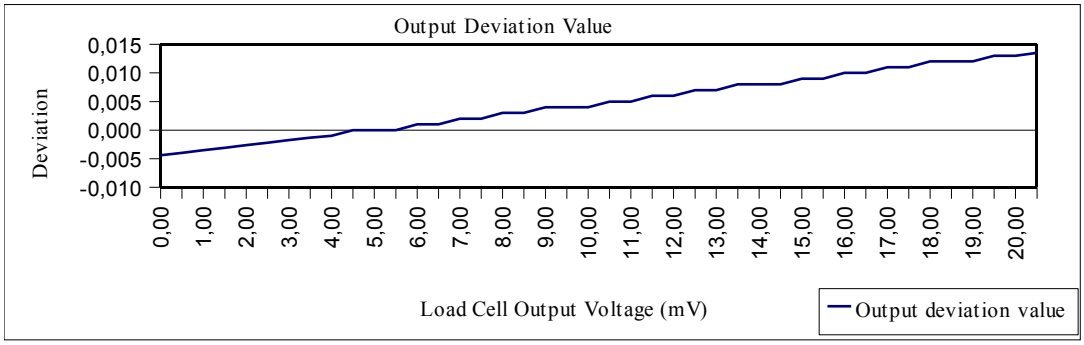

Figure 8. Output Deviation Value for Signal Conditioning

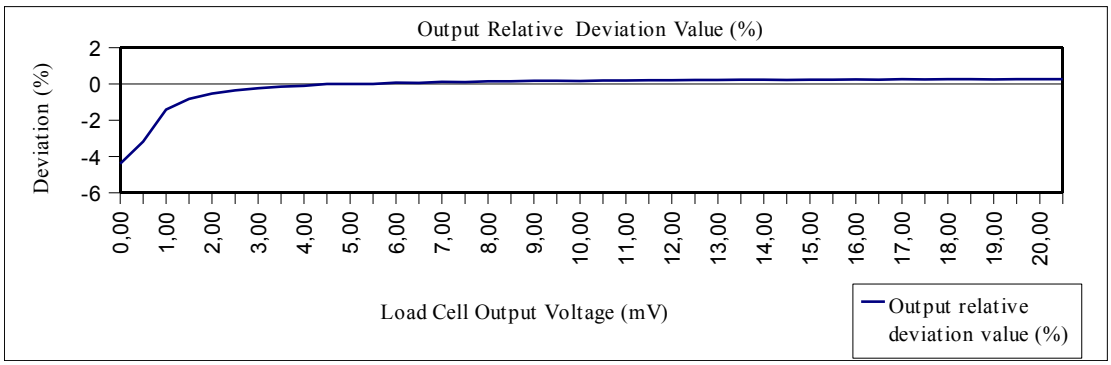

Figure 9. Output Relative Deviation Value in percentage for Signal Conditioning

However, the largest deviation found is 4,4%, and it is considered unsatisfactory for the values size of strength to be measured in the specimens test. But , it is occurred only for first part of scale range. This circuit is very simple and cheap and serves well the purpose of this application. It is clear that circuits more precisely and error less are desired. But, at this moment this one is sufficient. We are designing a circuit using a differential input stage, therefore more stable and adjusted to this case. This conditioning circuit will be based on AD8253 programmable gain instrumentation amplifier developed by Analog Devices™.

No tests were carried out with the load cell jointly the signal conditioning circuit motivated for lack of a testing machine that would apply across the range of forces required. Another problem concerns the fact that the construction of LSSF was not completed on time. The LSSF and DSAET are being developed separately during this stage of the research. However, the results of simulations are considered satisfactory for the purpose of functional analysis.

2.3. Signal Acquisition Board

The signal acquisition system is the one responsible for bridging the 0-20mV signal that comes from the load cell, which was converted to a 0-5V signal by the signal conditioning, and the PC/software, that will then analyze this input and plot it on a graph on the screen.

Figure 10. MC9S08AW60 board

The hardware responsible for this task is a MC9S08AW60 board, showed in Fig. 10. This board is the implementation of the MC9S08AW60 microcontroller, permitting it to be used for numerous applications. In Summerville, 2008, can be encountered some statements about this microcontroller. This board was developed by professor Denardin, at Industrial Automation Research Group and presents the following features:

a) 63.280 bytes of Flash Memory and 2048 bytes of RAM memory;
b) 16-channels, 10-bit AD (Analog-to-Digital) converters;
c) Inter-Integrated Circuit (IIC) bus module operating at up to 100 kbps with maximum bus loading;
d) 8-pin Keyboard Interruption;
e) 02 Serial Communications Interface (SCI);
f) One 2-channel and one 6-channel 16-bit timer/pulse-width modulator (TPM) module;
g) Up to 54 general-purpose input/output (I/O) pins;

h) Utilizes a 4-MHz external crystal to achieve 20-MHz internal bus frequency;
i) 0-5V source voltage.

The connection between the board and the PC used for Signal Analysis is made through a default serial cable at the rate of 57600 bauds. The protocol of communication between board and PC consists of a 3-byte series of commands sent from the PC to control the Board Actions and ask for the input signal from, which is being read through one of the AD channels. The protocol can be described as follows:

a) First Byte: identifies which action the board is intended to do, such as: define sampling rate, buffer size, each conversion channel state, acquire simple data channel, acquire buffered data channel or activate/deactivate buffered conversion;
b) Second Byte: acts as a modifier on almost all the actions determined by the first byte. It identifies which channel will receive the action, which buffer will receive the action and on the specific case of sampling rate time definition it acts as part of the desired time value, as in Eq. (4):

$$x = \left[\left(tempo\mu S * 20 \right) / 256 \right] (\text{int}) \tag{4}$$

c) Third Byte: acts as the value on almost all the actions described above, when it is necessary. Still, it must be always sent to complete protocol request, even if it doesn't have any meaning to the action selected.

The "Tab. 2" describes the 2nd and 3rd bytes function, according to the action set on the 1st byte.

Table 2. 2nd and 3rd byte functions compared to the action selected.

1st byte value	Action	2nd byte function	2nd byte possible values	3rd byte function	3rd byte possible values
1	Sampling rate time setup	Part of the value to be defined	$x = \left[\left(tempo\mu S * 20 \right) / 256 \right] (\text{int})$	Part of the value to be defined	$x = \left[\left(tempo\mu S * 20 \right) \%256 \right] (\text{int})$
2	Buffer size setup	Identifies which buffer	1-4	Desired value	0-255
3	Channel state setup	Identifies which channel	0-7	Identifies if it is active or not	255 = activated 0 = deactivated
4	No Function	-	-	-	-
5(2)	Simple channel acquisition	Identifies which channel	0-3	Not used	-
6(2)	Buffered channel acquisition	Identifies which channel	1-4	Not Used	-
7	Activate/ Deactivate cyclic buffer capture	Identifies if it is active or not	0 = activated Other value = deactivated	Not Used	-
8	Activate/ Deactivate trigger activated capture	Identifies if it is active or not	0 = activated Other value = deactivated	Trigger Value	0-255

(2): This function sends data to the board. As it can only sent 1 byte at a time, firstly is sent de higher part and then the lower part.

The AD converter system present in the board, as presented by Freescale (2006), possesses 10-bit precision and operates thorough successive approximation technique. This converter was projected to support up to 20 separate analog inputs, however only 18 are implemented on the MC9S08AW series.

Following the protocol requisition for data, the board will execute the AD conversion differently according to the action requested, and will return to the PC a numeric code that can be defined as total points. Each point is equivalent to 0,00488V of the input signal and its total, equals the input signal 10-bit approximated value. This value is then sent to the PC split into 2 bytes, being the higher part sent first.

After the transition of data is done, the PC software will manipulate the data as it's intended for analysis, and the protocol communication is complete. To request another reading, the PC will have to make another requisition, for the process to begin again.

2.4. Application Software

When the load cell signal, properly converted from it's original value to a 0-5V signal, reaches the acquisition system, it's time for the software for signal analysis to collect this info, register, convert and provide ways for a human to interact with the data, providing a group of options and visual aids.

Written using the C# programming language (SOLIS, 2008), and based on the .NET Framework architecture, the signal analysis software consists of a main screen Fig. 11 that shows a graph component, information about the serial port setup, the protocol setup and the process of acquiring data and several options for data manipulation.

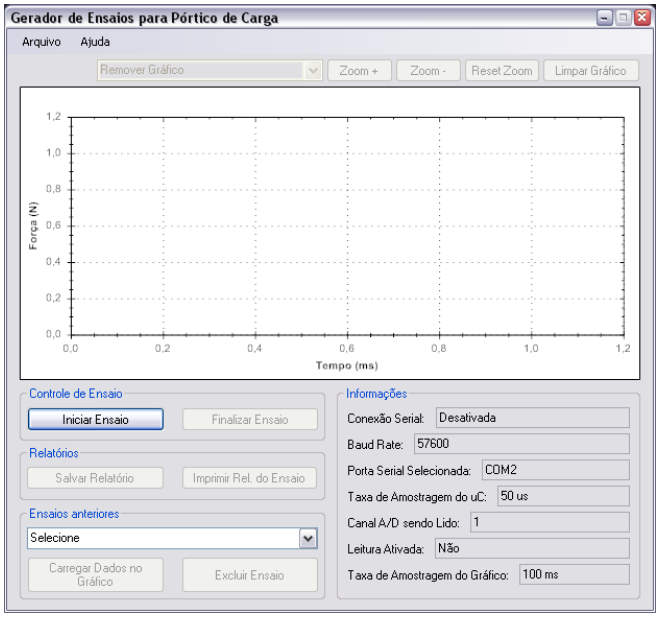

Figure 11. The "Gerador de Ensaios para Pórtico de Carga" – Signal Analysis Software

Besides the immediately seen options on the main screen, the software permits almost full control of the connection between the PC and the MC9S08AW60 board, and the characteristics of the test to be executed on the LSSF, through the two independent windows present on the *"Arquivo"* menu.

The *"Configurção da Porta Serial"* dialog Fig. 12 permits the user to configure which port of the PC the Software will use for connection with the acquisition system, as well as the reading and writing max time of the serial port. The *"Configuração do Ensaio"* dialog, shown in the Fig. 13 permits the configuration of several test-related options, such as: Channel to be acquired, Sampling Rate (can't be lower than 25ms) and Folder to which the Reports generated from each test will be saved.

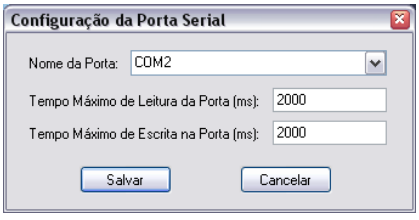

Figure 12. Dialog called by the *"Configuração da Porta Serial"* menu

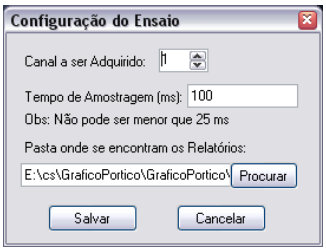

Figure 13. Dialog called by the *"Configuração do Ensaio"* menu

After the configurations are all set for the software to work properly, the process of testing becomes as easy as a one-button click. The user just has to click on the *"Iniciar Ensaio"* button, and the software will start to collect information from the load cell, plotting it on the graph Fig. 14. This doesn't mean the LSSF will start acting on the test body. The controls for the actuator are independent from the software and must be manually activated for it to work.

To finish the test, the user must press the *"Finalizar Ensaio"* button. This will stop the communication between PC and acquisition board, process the data acquired one last time and mark the Maximum Point of Force during the test on the graph. It will then enable the buttons for Saving a Report of the Test, or print the Report directly.

Another important function of the software is its ability to plot several Reports on the graph, along with a new test, or not Fig. 14. This provides the possibility comparison between two or more tests.

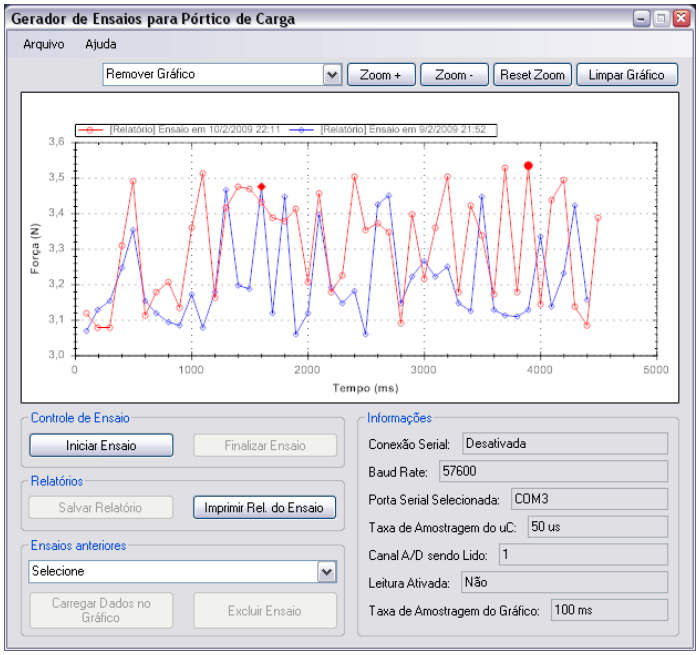

Figure 14. Multiple overlaid tests

There are still a set of tools for zooming and controlling the reports loaded in the graph that permit a better understanding on the differences between the forces measured on the tests. For a better visualization of the real values of each point in the graph, hovering them Fig. 15 with the mouse permits the user to see the Force and Time numeric values of that point.

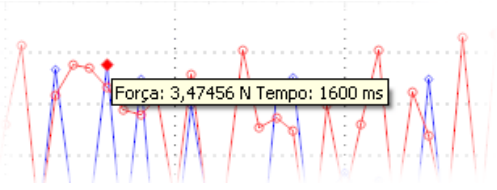

Figure 15. Force and Time values of a point tooltip

Finally, it is important to state that this software, being developed utilizing the.NET framework, will only work on Operational Systems where the framework is available, meaning mostly all Windows® releases.

3. CONCLUSIONS AND FUTURE ACKNOWLEDGEMENTS

This section discusses the research conclusions and potential future works that could improve the new equipment. From LSSF, it is hoped to develop new methods and techniques for the construction industry.

The signal conditioning circuit had good results considering aspects such as low cost and its expected functionality. But, future topology of conditioning circuit is provided to minimize the output deviation.

Testing the circuit with the conditioner along with the load cell was unable due to lack of machinery suitable for testing the magnitude of the forces to be measured. However, workbench tests were performed in which the output of the load cell (0-20mV) was applied at intervals of 0.5 mV, from 0mV to 20mV, for sale generally the efficiency of the circuit for signal conditioning.

The signal-conditioning circuit was also simulated and the load cell output voltage was replaced by the voltage source output. The results were very close to the work bench measured results replacing the load cell by a voltage source.

Considering 60.000kg of full-scale and signal-conditioning circuit maximal output deviation of 4,4%, at the beginning of the scale, this is the best fit curve of the output signal-conditioning circuit. This was considered satisfactory for the types of specimens' tests to be performed in LSSF for the moment.

The signal acquisition board has an error of signal conversion and propagation that can be considered negligible. Thus, the total error of the measuring system can be expressed in terms of load cell displacement deviation, that can be minimized by adjusting the offset of the load cell output voltage, therefore, depending on the adjustment made, may also be considered negligible. Thus, the total systematic deviation for the system is reduced to the signal-conditioning circuit deviation.

There was no study of systematic and random errors into the system, due to the LSSF not completely ready. This type of error has merits to the environment where the system we are characterizing the error, therefore, impossible to be reproduced in workbench. It is need the LSSF and DSAET coupled and are ready to begin the procedures for calibration of measuring system. In this stage, one appropriate method of statistical analysis must be used. Thus, it can be characterize a curve of error for the total system, taking into account the random and systematic errors of all DSAET modules. Furthermore, another system must be used as standard for calibration.

Once known the curve of error, the results of measurement can be represented with greater accuracy and precision.

Finally, this research should enter into its final stage soon, where the calibration procedure will be performed and work completed.

4. ACKNOWLEDGEMENTS

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